In the Claims:

Please amend claims 1 and 2. Please add new claims 22-25. The claims are as follows:

Claim 1. (Currently Amended) A semiconductor device comprising:

a substrate;

at least one fuse embedded within an interior portion of the substrate;

a continuous etch resistant layer on an exterior surface of the substrate, wherein the etch resistant layer is directly over an entire surface of the at least one fuse, and wherein the etch resistant layer is in direct mechanical contact with the at least one fuse; and

at least one insulative layer directly above the etch resistant layer, wherein the etch resistant layer has a slower etch rate than that of the at least one insulative layer thereabove.

Claim 2. (Currently Amended) The semiconductor device of claim 1, further comprising an alignment mark formed on the substrate at a location spatially removed from the fuse, wherein the alignment mark is adapted to provide an optical target for a laser.

Claim 3. (Original) The semiconductor device of claim 2, wherein the alignment mark further comprises the etch resistant layer thereover.

Claim 4. (Original) The semiconductor device of claim 2, wherein the fuse and the alignment mark are formed within a metal wiring layer of the device.

Claims 5 and 6 (Canceled)

Claim 7. (Original) The semiconductor device of claim 1, wherein the etch resistant layer comprises silicon nitride.

Claim 8. (Original) The semiconductor device of claim 1, wherein the etch resistant layer has a thickness of approximately 10-100 nm.

Claim 22. (New) The semiconductor device of claim 1, wherein the substrate comprises at least one metal wiring layer within the substrate, and wherein a first region of the metal wiring layer comprises the fuse.

Claim 23. (New) The semiconductor device of claim 22, wherein a plurality of remaining regions of the metal wiring layer are electrically connected to contact pads.

Claim 24 (New) The semiconductor device of claim 1, wherein the exterior surface of the substrate is coplanar with the entire surface of the at least one fuse.

Claim 25 (New) The semiconductor device of claim 2, wherein the substrate comprises at least one metal wiring layer within the substrate, wherein a first region of the metal wiring layer comprises the fuse, and wherein a second region of the metal wiring layer comprises the alignment mark.